AMENDMENTS TO THE SPECIFICATION

Please replace the first full paragraph on page 11 of the specification with the following amended paragraph.

Figure 5 shows clock circuit 113 which is a part of the core [[10]]. In includes a phase locked loop 54 which generates a first signal of 533 MHz and an inverse of the same signal. The first of these signals is also fed to a divide by eight circuit 56 so as to produce a 66 MHz clock signal. The first signal is processed to form the DCK signal. Depending on the mode in which the device is placed, the SCK signal is generated which is 180° out of phase with the DCK signal as indicated above. In other modes, the SCK and DCK signals are identical. The third signal is used as a 66 MHz signal as described in Fig. 2.